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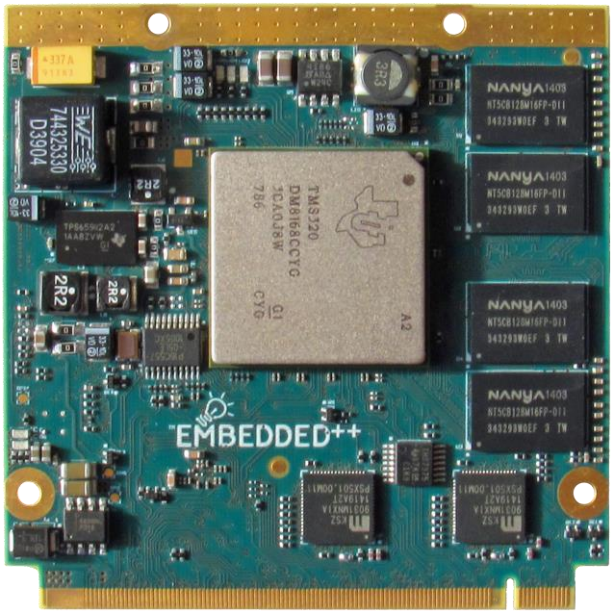


EPP-V7-DM8168™

Based on Texas Instruments® DaVinci™ TMS320DM8168

User Manual

for hardware revision 1.0

Document revision 1.2 (December 24th, 2014)

Preface

Important Information

This documentation is intended for qualified audience only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

Disclaimer

Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided “as is” and is subject to change without notice.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her owns expense.

Trademarks

All used product names, logos or trademarks are property of their respective owners.

Content

1 General Information

1.1 Revision History

Rev.	Date	Pages	Description
1.0	2014.07.31	All	• Initial version.
1.1	2014.10.15	18 18 18 23-28	• Updated description of V7_MODE# signal. • Removed UART0_RTS# and UART0_CTS# signals. • Added a notice about signal behaviour in Qseven® mode. • Updated signal types for Qseven®-compatibility mode.
1.2	2014.12.23	1 23-27	• Updated module picture. • Updated pin-out table layout.

1.2 Reference Documents

[1] Qseven ® Specification 2.0
http://www.qseven-standard.org

1.3 Signal Terminology

- Signal direction: Signal directions are from the module perspective.
  For example: COM_TXD (serial port transmit) is an output from the module.

- The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is active at a high voltage level.

- Differential pairs are indicated by trailing "+" and "-" signs for the positive or negative signal.

1.4 Introduction

The EPP-V7-DM8168™ is part of IMPT's Qseven®-compatible COM module family. It is based on Texas Instruments® DaVinci™ TMS320DM8168 System-on-a-Chip (SoC), incorporating a high-performance 32-bit ARM® Cortex-A8 RISC RISC MPU, 32-bit TMS320C674x floating-point VLIW DSP core, and three high-definition video codec engines based on ARM® Cortex-M3.

The module is mostly compliant with the Qseven® Specification revision 2.0, in terms that it can be safely evaluated on a Qseven®-compliant carrier board (the functional difference is listed in the MXM Connector Pin-out section). However, in order to utilize the complete capabilities, including built-in video input and output ports, and both Ethernet interfaces, a special carrier board is required. IMPT offers EPP-V7-CB™, the reference V7 carrier board for evaluation and a starting point for customizations.

The EPP-V7-DM8168™ module is available in 1 or 2 GBytes of DDR3 memory variants, in both industrial and commercial temperature range.

2 Technical Information

2.1 Key features(1)

CPU	ARM® Cortex-A8 RISC processor operating at 1.2 GHz ■ 32KB instruction and data caches ■ 256KB L2 cache ■ 64KB RAM, 48KB boot ROM C674x floating/fixed point DSP operating at 1 GHz ■ Up to 8000/6000 C674x MIPS/MFLOPS
Memory	Dual 32-bit DDR3 SDRAM at 800 MHz (1600 MT/s), 1 or 2 GBytes
HD Video Processors	Three HDVICP2 Cortex-M3 based hardware engines supporting encoding & decoding video in resolutions up to 1080p60. ■ MPEG1, MPEG2, MPEG4 (ASP and SP) ■ H.264 (BL, MP and HP) ■ VC-1 (SP, MP and AP) ■ RV9 and RV10 ■ AVS 1.0 ■ ON2 (VP6.2 and VP7)
Video outputs	■ One digital HDMI 1.3 transmitter with HDCP, up to 1080p60 ■ One 16-bit paralel video output port (supporting YCbCr and BT.656 modes up to 165 MHz) with separate HSync/VSync signals, allowing embedded and discrete sync modes ■ One SD analog output with separate Y/C channels, compatible with S-video standard
Video inputs	■ One 24-bit paralel video input port (up to 165 MHz) with separate HSync/VSync signals, supporting single-channel 16-bit/24-bit (YCbCr and RGB) video with embedded or discrete sync, or dual-channel 8-bit (YCbCr) with embedded sync ■ One 16-bit paralel video input port (up to 165 MHz) with separate HSync/VSync signals, supporting single-channel 16-bit (YCbCr) video with embedded or discrete(2) sync, or dual-channel 8-bit (YCbCr) video with embedded sync
GPU	SGX530 3D Graphics Engine ■ Delivers up to 30 MTriangles/s ■ Compatible with OpenGL ES 1.1/2.0 and OpenVG v1.1
Ethernet	Dual Micrel KSZ9031MNX Ethernet PHY, IEEE 802.3 compliant (full duplex 10Base-T/100Base-TX/1000Base-T)
PCI Express	One PCI Express Gen2 dual-lane port

Audio	One Texas Instruments McASP port, I2S-compatible(3)
USB	Dual USB 2.0 Controller (supports host and client modes)
SATA	Dual SATA 3.0 Gbps interface
Serial, SPI, I²C	■ Two UART ports (one with RTS/CTS flow control, one supporting TX/RX only and multiplexed with JTAG port) ■ SPI controller up to 40 MHz (two chip selects available on the connector) ■ Two I²C ports supporting 100 kHz and 400 kHz modes
Flash Memory	■ 8-bit NAND Flash, 2 GByte capacity ■ SPI Flash, 4 MB capacity
SDIO	4-bit SD/MMC Controller supporting 2.00 specification (High-Speed), up to 48 MHz
RTC	RTC via I²C-Interface (typical power consumption 350 nA @ 3V)
Temperature sensor	Connected to the power management module
Boot sources(4)	■ SD card ■ SPI Flash
Package	1031-Pin Pb-Free BGA Package, 25,2x25,2mm, 0,65mm pitch, 2,81mm max. height.
Power Supply	5V (4,75V – 5,25V) 5V (4,75V – 5,25V) standby voltage 3V (1,3V – 3,3V) optionally for RTC

[1] Features listed in this table are fully available only in V7 mode. Features disabled in Qseven®-compatibility mode are listed in a separate table.

[2] Due to pin multiplexing in the chip, HSync/VSync pins for the second (16-bit) video input port are shared with data signals in the upper octet of the first (24-bit) input port. If the first port is used in full 24-bit mode, discrete sync is not available for the second port.

[3] It is highly recommended to use McASP compatible audio codecs (such as TLV320AIC310x family) on the carrier board, due to better software support in Linux operating system.

[4] U-Boot bootloader must be installed in onboard SPI Flash or the SD Card. When U-Boot is loaded and executed, main operating system can be loaded over Ethernet.

2.2 Jumpers and switches

There are no jumpers or switches available on the module.

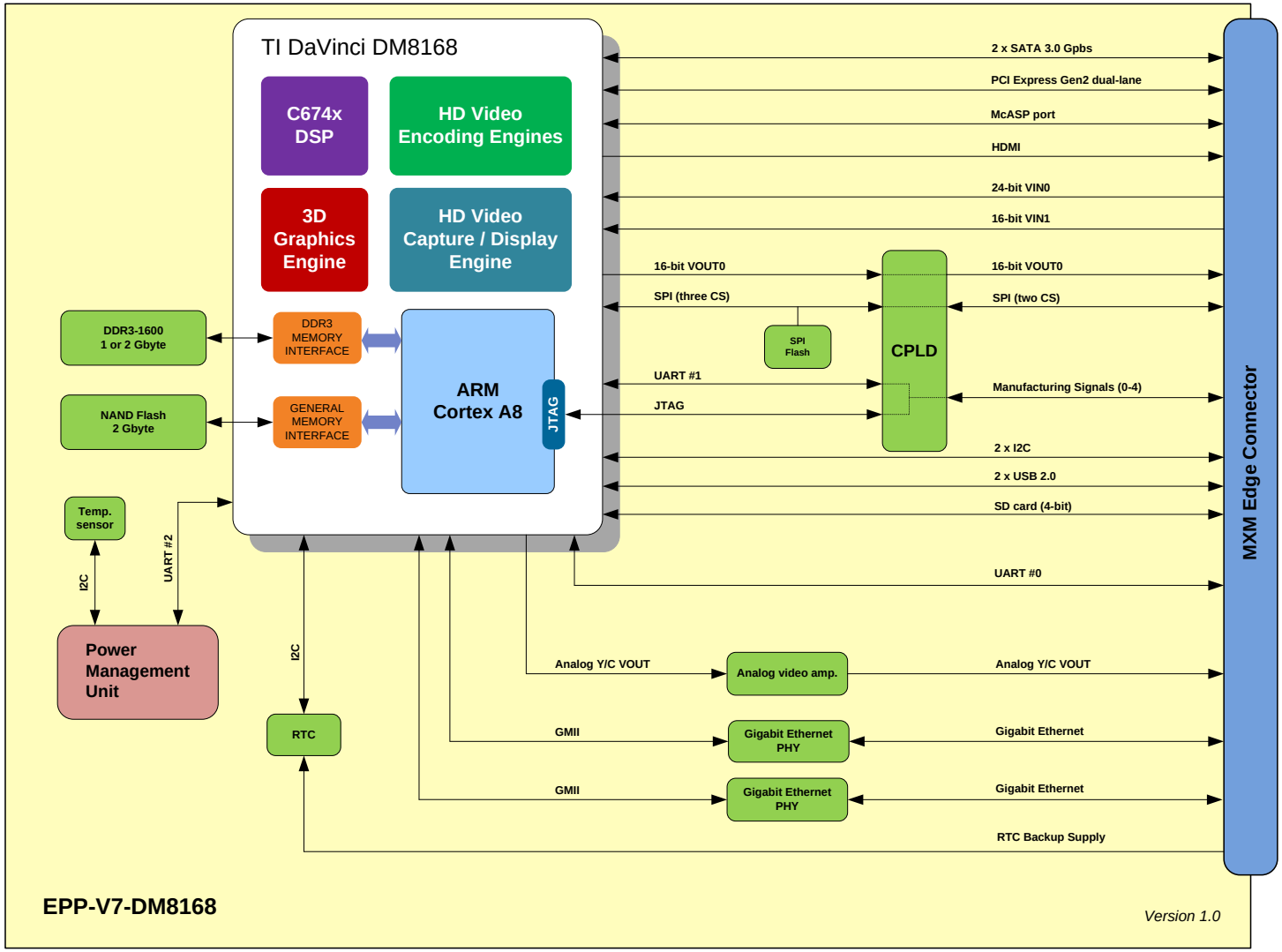
2.3 Watchdog

External watchdog is not supported in current software distribution, since DM8168 has a built-in watchdog.

2.4 Power dissipation

Mode	Voltage	Current	Power	Description
Idle	5V	TBD	TBD	Measured at the login prompt ten minutes after booting
CPU tests	5V	TBD	TBD	Measured while running CPU tests fifteen minutes after booting
HD video	5V	TBD	TBD	Measured while decoding HD video (hardware accelerated) two minutes after rebooting

2.5 Block diagram



2.6 LED Indication

There are three onboard LEDs controllable by software and available for user application. However, in normal operation they are covered by heatsink and are not visible from the outside. Please consult the BSP manual for instructions how to control them in Linux operating system.

2.7 Signal Description (V7 Mode)

In the following table, signals are marked with the power rail associated with the pin, and with the input voltage tolerance (for input and I/O pins). The pin power rail and the pin input voltage tolerance maybe different.

2.7.1 PCI Express Lanes

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
PCIE0_TX+ PCIE0_TX-	O	PCIe	CPU	AC coupled on module		PCI Express Gen2 differential transmit pairs 0.	DM8168
PCIE0_RX+ PCIE0_RX-	I	PCIe	CPU	Requires AC coupling on baseboard		PCI Express Gen2 differential receive pairs 0.	Exp. connector
PCIE1_TX+ PCIE1_TX-	O	PCIe	CPU	AC coupled on module		PCI Express Gen2 differential transmit pairs 1.	DM8168
PCIE1_RX+ PCIE1_RX-	I	PCIe	CPU	Requires AC coupling on baseboard		PCI Express Gen2 differential receive pairs 1.	Exp. connector
PCIE_CLK_REF+ PCIE_CLK_REF-	O	PCIe	CPU	AC coupled on module		PCI Express reference clock.	Onboard clock generator
PCIE_RST#	O	CMOS	CPU	3.3V		Reset signal output.	DM8168
PCIE_WAKE#	I	CMOS	CPU	3.3V		External wake signal input.	Exp. connector

2.7.2 Ethernet

<table>
<tr><th>Signal</th><th>Pin Type</th><th>Signal Level</th><th>Power Rail</th><th>Remark / Power Tol.</th><th>PU/PD</th><th>Description</th><th>Source</th></tr>
<tr><td>GBE0_MDI[0:3]+
GBE0_MDI[0:3]-
GBE1_MDI[0:3]+
GBE1_MDI[0:3]+</td><td>I/O</td><td>Ethernet MDI</td><td>CPU</td><td></td><td></td><td>Gigabit Ethernet Controller: Media Dependent Interface Differential Pairs 0, 1, 2, and 3. The MDI can operate in 1000Base-T, 100Base-TX and 10Base-T modes.

<u>1000BASE-T</u>
<table><tr><th colspan="2">MDI configuration:</th><th colspan="2">MDI-X configuration:</th></tr><tr><td>MDI[0]+/-</td><td>BI_DA+/-</td><td>MDI[0]+/-</td><td>BI_DB+/-</td></tr><tr><td>MDI[1]+/-</td><td>BI_DB+/-</td><td>MDI[1]+/-</td><td>BI_DA+/-</td></tr><tr><td>MDI[2]+/-</td><td>BI_DC+/-</td><td>MDI[2]+/-</td><td>BI_DC+/-</td></tr><tr><td>MDI[3]+/-</td><td>BI_DD+/-</td><td>MDI[3]+/-</td><td>BI_DD+/-</td></tr></table>
<u>100BASE-TX/ 10BASE-T</u>
<table><tr><th colspan="2">MDI configuration:</th><th colspan="2">MDI-X configuration:</th></tr><tr><td>MDI[0]+/-</td><td>Transmit</td><td>MDI[0]+/-</td><td>Receive</td></tr><tr><td>MDI[1]+/-</td><td>Receive</td><td>MDI[1]+/-</td><td>Transmit</td></tr><tr><td>MDI[2]+/-</td><td>unused</td><td>MDI[2]+/-</td><td>unused</td></tr><tr><td>MDI[3]+/-</td><td>unused</td><td>MDI[3]+/-</td><td>unused</td></tr></table></td><td>Ethernet PHY</td></tr>
<tr><td>GBE0_ACT#
GBE1_ACT#</td><td>O</td><td>CMOS</td><td>CPU</td><td>3.3V</td><td></td><td>Gigabit Ethernet Controller: activity indicator, active low.</td><td>Eth PHY</td></tr>
<tr><td>GBE0_LINK#
GBE1_LINK#</td><td>O</td><td>CMOS</td><td>CPU</td><td>3.3V</td><td></td><td>Gigabit Ethernet Controller: link indicator, active low.</td><td>Eth PHY</td></tr>
<tr><td>GBE0_LINK100#
GBE1_LINK100#</td><td>O</td><td>CMOS</td><td>CPU</td><td>3.3V</td><td></td><td>Gigabit Ethernet Controller: 100 Mbit mode indicator, active low.</td><td>DM8168</td></tr>
<tr><td>GBE0_LINK1000#
GBE1_LINK1000#</td><td>O</td><td>CMOS</td><td>CPU</td><td>3.3V</td><td></td><td>Gigabit Ethernet Controller: 1000 Mbit mode indicator, active low.</td><td>DM8168</td></tr>
<tr><td>GBE0_CTREF
GBE1_CTREF</td><td>NC</td><td></td><td></td><td>GND min
3.3V max</td><td></td><td>Gigabit Ethernet Controller: unconnected</td><td>Not connected</td></tr>
</table>

2.7.3 Serial ATA Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
SATA0_TX+ SATA0_TX-	O	SATA	CPU	AC coupled on module		Serial ATA Channel 0: differential transmit pair.	DM8168
SATA0_RX+ SATA0_RX-	I	SATA	CPU	AC coupled on module		Serial ATA Channel 0: differential receive pair.	Exp. connector
SATA1_TX+ SATA1_TX-	O	SATA	CPU	AC coupled on module		Serial ATA Channel 1: differential transmit pair.	DM8168
SATA1_RX+ SATA1_RX-	I	SATA	CPU	AC coupled on module		Serial ATA Channel 1: differential receive pair.	Exp. connector
SATA_ACT#	OD Output	CMOS	CPU	3.3V		SATA activity indicator (mutual for both channels), active low. An external pull-up needs to be installed on the carrier board.	DM8168

2.7.4 USB Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
USB_P0+ USB_P0-	I/O	USB	CPU			USB differential pair, channels 0.	DM8168 or exp. connector
USB_P1+ USB_P1-	I/O	USB	CPU			USB differential pair, channels 1.	DM8168 or exp. connector
USB_0_1_OC#	I	CMOS	CPU	3.3V	1k43 PU	USB over-current sense for both USB channels. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. **Do not pull this line high on the carrier board.**	Exp. connector
USB_ID	I	CMOS	CPU	3.3V		USB ID pin. High signal level can be used in software to configure USB Port 0 or 1 as USB client.	Exp. connector
USB_CC	I	CMOS	CPU	3.3V		USB client connect pin.	Exp. connector

2.7.5 SDIO Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
SDIO_DAT[0:3]	I/O	3.3V	CPU	3.3V	10k PU	SDIO data lines.	DM8168 or exp. connect.
SDIO_CD#	I	3.3V	CPU	3.3V		SDIO card detect signal.	Exp. connector
SDIO_CMD	I/O	3.3V	CPU	3.3V	10k PU	SDIO command line.	DM8168 or exp. connect.
SDIO_CLK	O	3.3V	CPU	3.3V	10k PU	SDIO clock line.	DM8168
SDIO_PWR#	I/O	3.3V	CPU	3.3V	10k PU	SDIO power enable signal.	DM8168 or exp. connect.
SDIO_LED	O	3.3V	CPU	3.3V	10k PD	SDIO transfer activity LED.	DM8168
SDIO_WP	I	3.3V	CPU	3.3V		SDIO write protect signal.	Exp. connector

2.7.6 Audio Interface (McASP Port, I^2S Compatible)

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
I2S_RST#	Output	CMOS	CPU	3.3V	10k PD	Reset output to carrier board's audio codec, active low.	DM8168
I2S_WS / MCA2_AFSX	Output	CMOS	CPU	3.3V		I2S word select clock to codec (WCLK for codecs with McASP interface).	DM8168
I2S_CLK / MCA2_ACLKX	Output	CMOS	CPU	3.3V		I2S bit clock to codec (BCLK for codecs with McASP interface).	DM8168
I2S_SDO / MCA2_AXR1	Output	CMOS	CPU	3.3V		Serial data output to codec.	DM8168
I2S_SDI / MCA2_AXR0	Input	CMOS	CPU	3.3V		Serial data input from codec.	Exp. connector
MCA2_AHCLKX	I/O	CMOS	CPU	3.3V		MCLK for codecs with McASP interface.	DM8168 or exp. connect.

2.7.7 HDMI Output

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
DP_LANE2+/TMDS_LANE0+ DP_LANE2-/TMDS_LANE0-	O	HDMI	CPU			TMDS differential pair lines, lane 0.	DM8168
DP_LANE1+/TMDS_LANE1+ DP_LANE1-/TMDS_LANE1-	O	HDMI	CPU			TMDS differential pair lines, lane 1.	DM8168
DP_LANE0+/TMDS_LANE2+ DP_LANE0-/TMDS_LANE2-	O	HDMI	CPU			TMDS differential pair lines, lane 2.	DM8168
DP_LANE3+/TMDS_CLK+ DP_LANE3-/TMDS_CLK-	O	HDMI	CPU			TMDS differential pair lines, clock.	DM8168
DP_HDMI_HPD#	I	CMOS	CPU		10k PD	Hot-plug detection signal that serves as an interrupt request line. Signal can be pulled only to a logic low level.	Exp. connector
HDMI_CTRL_CLK	I/O OD	CMOS	CPU	3.3V	40k2 PU	DDC based control signal (clock) for HDMI device.	DM8168
HDMI_CTRL_DAT	I/O OD	CMOS	CPU	3.3V	40k2 PU	DDC based control signal (data) for HDMI device.	DM8168

2.7.8 SPI Interface

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
SPI_MOSI	O	CMOS	CPU	3.3V		Master serial output.	DM8168
SPI_MISO	I	CMOS	CPU	3.3V		Master serial input / Peripheral serial output.	Exp. connector
SPI_SCK	O	CMOS	CPU	3.3V		SPI clock output.	DM8168
SPI_CS0#	O	CMOS	CPU	3.3V	5k1 PU	The second[1] SPI chip select output, active low.	DM8168
SPI_CS1#	O	CMOS	CPU	3.3V	5k1 PU	The third[1] SPI chip select output, active low.	DM8168

[1] First SPI chip select signal is reserved for access to onboard SPI Flash memory.

2.7.9 Input Power Pins

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
VCC	Power		5V	(±5%)		Primary power input towards voltage regulators: +5V (±5%).	Exp. connector
VCC_5V0_SB	Power		5V	(±5%)		Standby power input towards voltage regulators: +5.0V (±5%) All available VCC5V0_STBY pins on the connector(s) shall be used. Used for microcontroller and standby and suspend functions. ***NOTE: If no standby power is available, connect it to VCC5V0!***	Exp. connector
VCC_RTC	Power		Suspend			Real-time clock circuit-power input : +3.0V (+1.3V to +3.3V).	Exp. connector
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.7.10 JTAG / UART #1 Pins (Manufacturing Signals for Qseven®-compatibility mode)

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
MFG_NC0[(2)] / JTAG_TCLK	I	CMOS	CPU	3.3V		Boundary Scan – TCK	Exp. connector
MFG_NC1 / JTAG_TDO / UART1_TX	O	CMOS	CPU	3.3V		Boundary Scan – TDO / COM_TXD: Depending on MFG_NC4 level, the signal is either used as Boundary Scan TDO, or as transmit line for UART #1 port.	DM8168
MFG_NC2 / JTAG_TDI / UART1_RX	I	CMOS	CPU	3.3V		Boundary Scan – TDI / COM_RXD: Depending on MFG_NC4 level, the signal is either used as Boundary Scan TDI, or as receive line for UART #1 port.	Exp. connector
MFG_NC3 / JTAG_TMS	I	CMOS	CPU	3.3V		Boundary Scan – TMS.	Exp. connector
MFG_NC4[(3)] / JTAG_TRST# / MFG_SEL	I	CMOS	CPU	3.3V		Control Signal for multiplexer circuit: 1: Boundary Scan / JTAG 0: UART #1	Exp. connector

[2] On some JTAG debuggers which require a return clock from processor, pins TCK and RCK should be tied (pins 11 and 9 on standard Texas Instruments 14-pin JTAG Header).

[3] This signal should have a defined default logic level (using a pull-up or pull-down resistor on the carrier board).

2.7.11 Video Input Port 0

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
VIN[0]A_D[0:23]	I	CMOS	CPU	3.3V		Digital VIN0 port data lines. For 24-bit RGB capture, D[23:16] are red, D[15:8] are green, and D[7:0] are blue data bits. For 16-bit capture, D[7:0] are multiplexed Cb/Cr and D[15:8] are Y data bits for Port A. For 8-bit capture, D[7:0] are multiplexed YCbCr data bits for Port A, and D[15:8] are multiplexed YCbCr data bits for Port B.	Exp. conn.
VIN[0]A_CLK	I	CMOS	CPU	3.3V		Input clock for 8-bit, 16-bit, or 24-bit Port A capture.	Exp. conn.
VIN[0]A_HSYNC	I	CMOS	CPU	3.3V		Discrete horizontal synchronization signal for Port A RGB capture, or YCbCr capture without embedded synchronization.	Exp. conn.
VIN[0]A_VSYNC	I	CMOS	CPU	3.3V		Discrete vertical synchronization signal for Port A RGB capture, or YCbCr capture without embedded synchronization.	Exp. conn.
VIN[0]A_FLD	I	CMOS	CPU	3.3V		Discrete field ID signal for Port A RGB capture, or YCbCr capture without embedded synchronization.	Exp. conn.
VIN[0]A_DE	I	CMOS	CPU	3.3V		Discrete data enable signal for Port A RGB capture, or YCbCr capture without embedded synchronization.	Exp. conn.
VIN[0]B_CLK	I	CMOS	CPU	3.3V		Input clock for 8-bit Port B capture. Not used in 16-bit and 24-bit capture modes.	Exp. conn.
VIN[0]B_HSYNC	I	CMOS	CPU	3.3V		Discrete horizontal synchronization signal for Port B 8-bit YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[23] and is not available for VIN[0]B_HSYNC functionality if VIN0 port is used for 24-bit capture.	Exp. conn.
VIN[0]B_VSYNC	I	CMOS	CPU	3.3V		Discrete vertical synchronization signal for Port B 8-bit YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[22] and is not available for VIN[0]B_VSYNC functionality if VIN0 port is used for 24-bit capture.	Exp. conn.
VIN[0]B_FLD	I	CMOS	CPU	3.3V		Discrete field ID signal for Port B 8-bit YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[21] and is not available for VIN[0]B_FLD functionality if VIN0 port is used for 24-bit capture.	Exp. conn.
VIN[0]B_DE	I	CMOS	CPU	3.3V		Discrete data enable signal for Port B 8-bit YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[20] and is not available for VIN[0]B_DE functionality if VIN0 port is used for 24-bit capture.	Exp. conn.

2.7.12 Video Input Port 1

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
VIN[1]A_D[0:15]	I	CMOS	CPU	3.3V		Digital VIN1 port data lines. For 16-bit capture, D[7:0] are Cb/Cr and D[15:8] are Y data bits for Port A. For 8-bit capture, D[7:0] are multiplexed YCbCr data bits for Port A, and D[15:8] are multiplexed YCbCr data bits for Port B.	Exp. conn.
VIN[1]A_CLK	I	CMOS	CPU	3.3V		Input clock for 8-bit or 16-bit Port A capture.	Exp. conn.
VIN[1]A_HSYNC	I	CMOS	CPU	3.3V		Discrete horizontal synchronization signal for Port A YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[16] and is not available for VIN[1]A_HSYNC functionality if VIN0 port is used for 16-bit or 24-bit capture.	Exp. conn.
VIN[1]A_VSYNC	I	CMOS	CPU	3.3V		Discrete vertical synchronization signal for Port A YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[17] and is not available for VIN[1]A_VSYNC functionality if VIN0 port is used for 16-bit or 24-bit capture.	Exp. conn.
VIN[1]A_FLD	I	CMOS	CPU	3.3V		Discrete field ID signal for Port A YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[18] and is not available for VIN[1]A_FLD functionality if VIN0 port is used for 16-bit or 24-bit capture.	Exp. conn.
VIN[1]A_DE	I	CMOS	CPU	3.3V		Discrete data enable signal for for Port A YCbCr capture without embedded synchronization. **NOTE:** This signal is multiplexed with VIN[0]A_D[19] and is not available for VIN[1]A_DE functionality if VIN0 port is used for 16-bit or 24-bit capture.	Exp. conn.
VIN[1]B_CLK	I	CMOS	CPU	3.3V		Input clock for 8-bit Port B video capture. Not used in 16-bit capture mode.	Exp. conn.

2.7.13 Video Output Ports

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
VDAC_Y	O	S-Video	CPU		PD, 37.4O	Luma (Y) component of the analog SD video output port.	Video amp.
VDAC_C	O	S-Video	CPU		PD, 37.4O	Chroma (C) component of the analog SD video output port.	Video amp.
VOUT[0]_CLK	O	CMOS	CPU	3.3V		Digital VOUT0 port, output clock.	CPLD
VOUT[0]_FLD	O	CMOS	CPU	3.3V		Digital VOUT0 port, discrete field ID output signal.	CPLD
VOUT[0]_HSYNC	O	CMOS	CPU	3.3V		Discrete horizontal synchronization signal (not used for embedded sync modes).	CPLD
VOUT[0]_VSYNC	O	CMOS	CPU	3.3V		Discrete vertical synchronization signal (not used for embedded sync modes).	CPLD
VOUT[0]_G_Y_YC[2:9]	O	CMOS	CPU	3.3V		Y (Luma) data bits for 16-bit YCbCr mode; Multiplexed YCbCr data bits for 8-bit BT.656 mode.	CPLD
VOUT[0]_B_CB_C[2:9]	O	CMOS	CPU	3.3V		Multiplexed CbCr (Chroma) data bits for 16-bit YCbCr mode; Unused for 8-bit BT.656 mode.	CPLD

2.7.14 Power and System Management

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source
V7_MODE#	Power (N/C)		5V	5V	10k PU	Carrier board detection signal. Used by the power management subsystem to detect carrier board type and automatically reconfigure the connector pin-out between V7 mode and Qseven®-compatibility mode. This signal is connected to 5V power rail on Qseven® carrier boards, but it must be left **disconnected** on V7-compliant carrier boards (otherwise, wrong carrier board detection will occur, which can damage the hardware).	Exp. connector (leave N/C on V7-compliant carrier boards)
PWRBTN#	I	CMOS	Suspend	3.3V	10k PU	Power button to bring system into a power state. Active low (negative pulse).	Exp. connector
RSTBTN#	I	CMOS	Suspend	3.3V	10k PU	Reset button input. System is held in hardware reset while this input is low, and comes out of reset upon release. Active low (negative pulse).	Exp. connector
SUS_S3#	O	CMOS	Suspend	3.3V	10k PD	Power management output which is used to switch the main power supply. Active low.	Power mgmnt. unit
WAKE#	I	CMOS	Suspend	3.3V	10k PU	External system wake up signal. Active low.	Exp. connector
PWGIN	I	5V CMOS	Suspend	5V		Indicates that the external power supply is ready.	Exp. connector
GP0_I2C_CLK	I/O	CMOS	CPU	3.3V	1k43 PU	General purpose I2C port 0 clock output.	DM8168
GP0_I2C_DAT	I/O	CMOS	CPU	3.3V	1k43 PU	General purpose I2C port 0 data line.	DM8168
GP1_I2C_CLK	I/O	CMOS	CPU	3.3V	5k1 PU	General purpose I2C port 1 clock output.	DM8168
GP1_I2C_DAT	I/O	CMOS	CPU	3.3V	5k1 PU	General purpose I2C port 1 clock output.	DM8168
EXT_INT1#	I	CMOS	CPU	3.3V		General purpose external interrupt source. Active low.	Exp. connector
EXT_INT2#	I	CMOS	CPU	3.3V		General purpose external interrupt source. Active low.	Exp. connector
UART0_TX	O	CMOS	CPU	3.3V		Transmit line for UART #0 port.	DM8168
UART0_RX	I	CMOS	CPU	3.3V	10k PU	Receive line for UART #0 port.	Exp. connector

NOTE: Please examine the pin-out difference between V7 mode and Qseven®-compatibility mode (listed in a separate section of this document), and also refer to Qseven® specification 2.0, which contains the exact description and nature of signals not listed in V7 signal description tables.

3 System resources

3.1 Boot options

The EPP-V7-DM8168™ supports multiple booting options. The bootloader ("U-Boot") can be loaded from SD card or the onboard SPI Flash memory. SD card boot is of higher priority than SPI Flash boot, which is useful for development and as a rescue method (when data on SPI Flash gets corrupted or accidentally overwritten). If an SD card is present in the system, but doesn't contain a valid bootloader, the CPU will skip to SPI Flash boot method.

When the U-Boot bootloader is loaded and started, Linux operating system can be loaded via Ethernet, NAND Flash, or SD Card. Please consult the Linux BSP manual for complete information about boot options.

3.2 I²C Bus Address Map

The following addresses are in use by I²C peripherals on the module, and should not be used for peripherals on the carrier board.

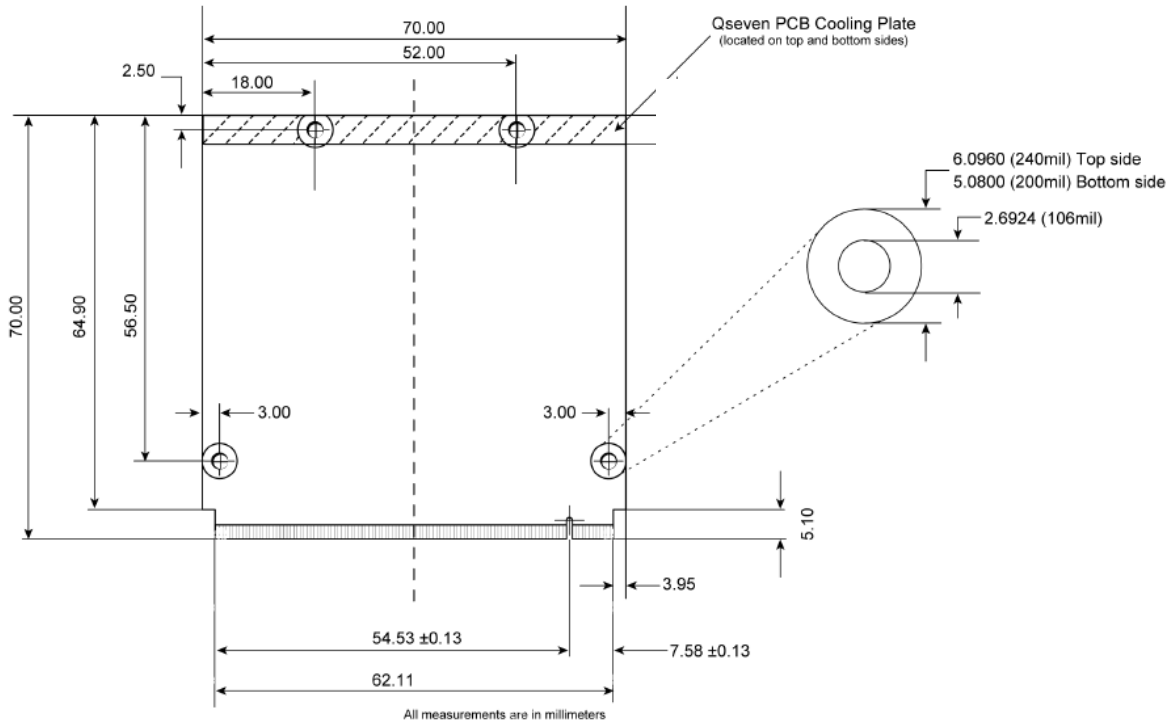
Device on Module	I²C Bus	A6	A5	A4	A3	A2	A1	A0	R/ W	Address (8-bit RW)	Adress in Linux
PMIC	0	0	1	0	1	1	0	1	x	$5A_h$ / $5B_h$	$2D_h$
RTC	0	1	1	0	1	0	0	0	x	$D0_h$ / $D1_h$	68_h

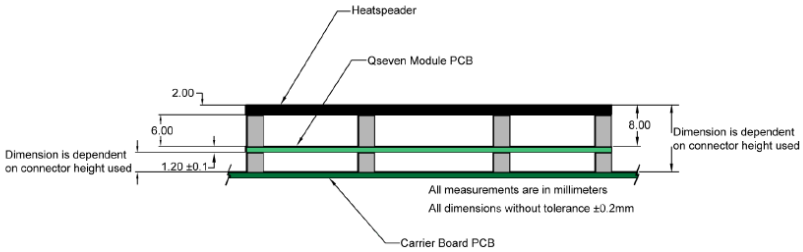
NOTES:

In default software configuration shipped with the module, audio codec on the carrier board (such as EPP-V7-CB™) is expected to have the address 18h on I²C bus 0 (not counting r/w bit, which is automatically set by the operating system depending on read or write request).

Multiple video capture and display controllers, and the controlling GPIO I²C expander, are expected at several addresses on I²C bus 1 when running default software configuration on the reference V7 carrier board (EPP-V7-CB™). Please consult the user manual for EPP-V7-CB™ for the list of exact addresses.

4 Mechanical drawing





The actual height depends on the MXM connector used on the baseboard.

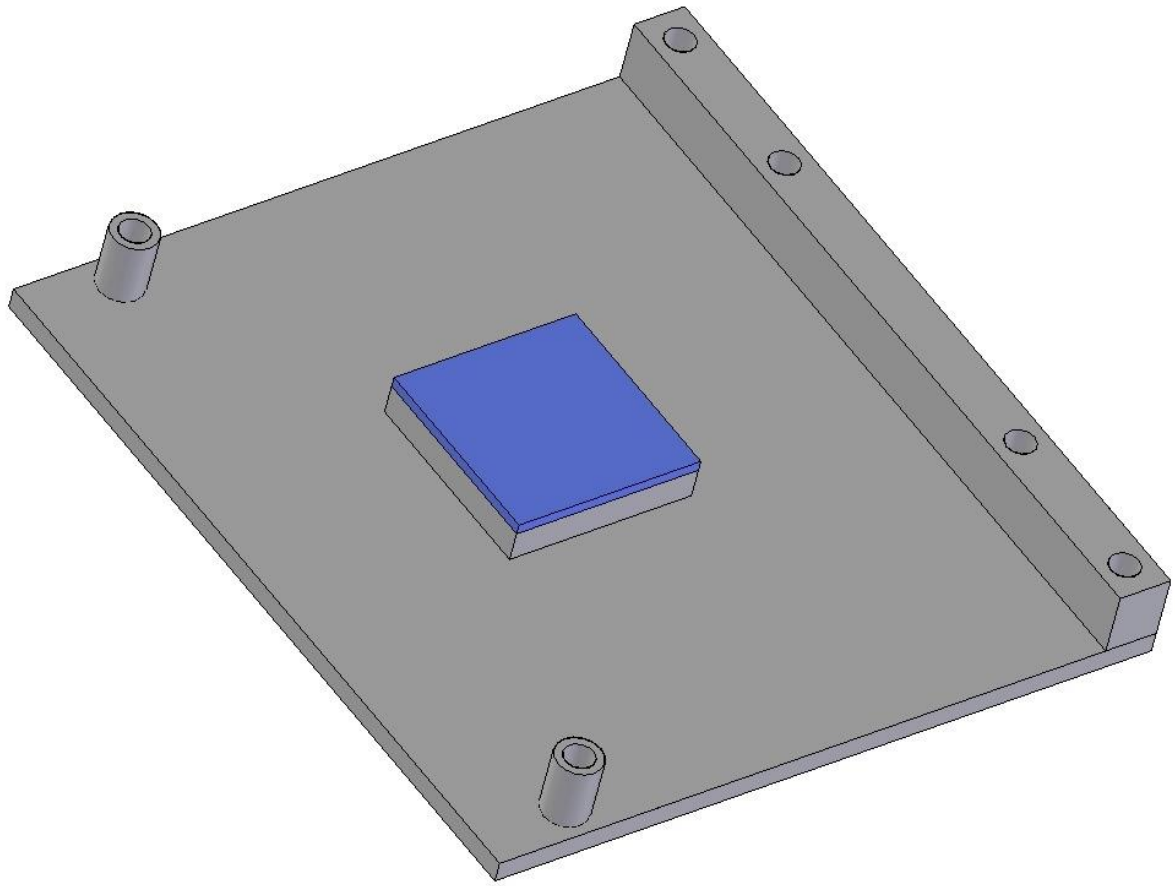
5 Heat spreader

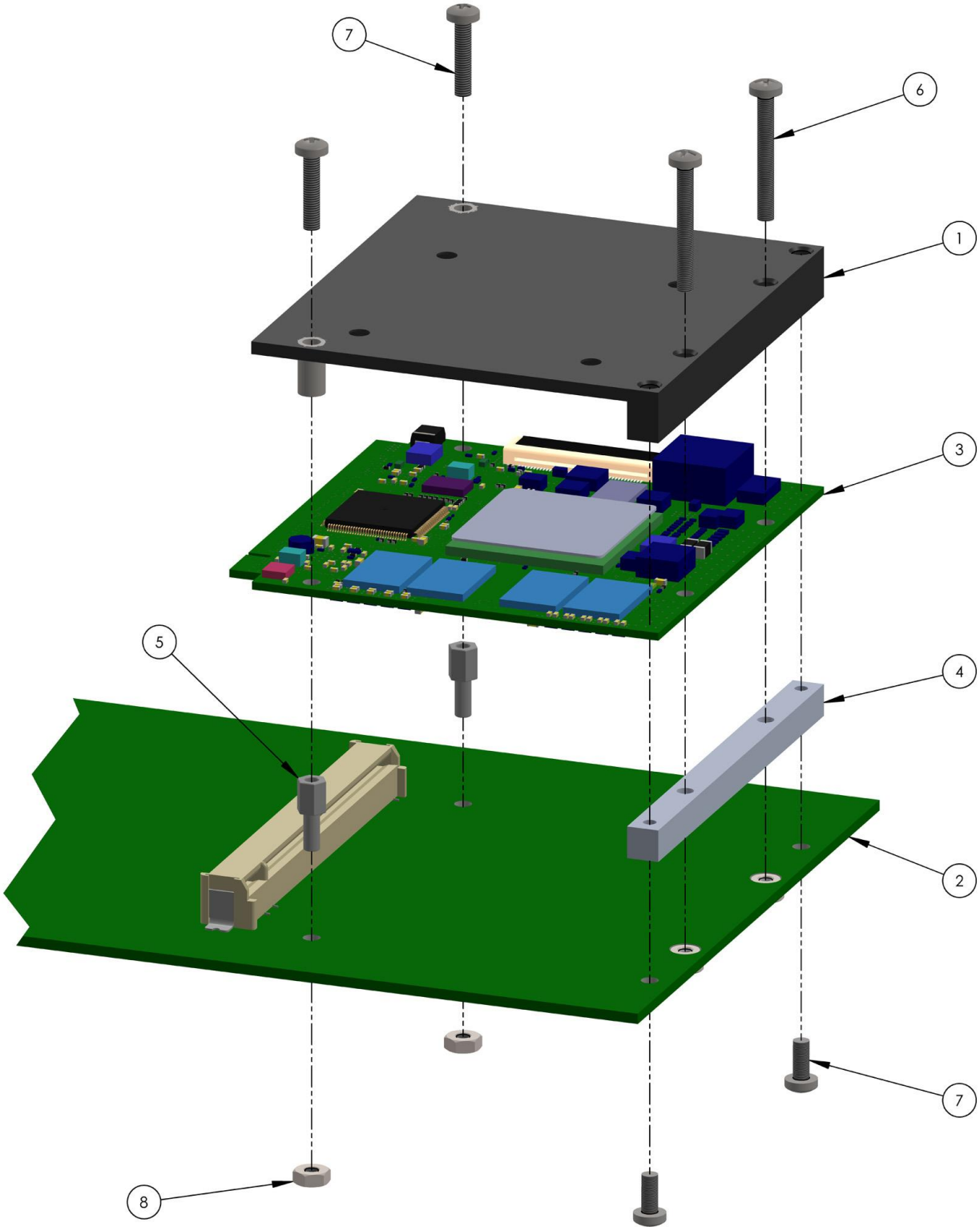
The EPP-V7-DM8168™ module uses a cooling solution for Qseven® module, which is based on a heat spreader concept. The purpose of the heat spreader is to provide a standard thermal interface.

A heat spreader is a metal plate (typically aluminium) mounted on top of the module. Its mechanical dimensions follow the module standard specification. The connection between the metal plate and the thermal active components on the module is typically made via thermal interface materials such as phase change foils, gap pads and metal blocks. A good thermal conductivity is required in order to transfer the heat from the hotspots to the heat spreader plate.

The heat spreader used for the EPP-V7-DM8168™ module is thermally attached using phase change materials and a small aluminium block that is part of the heat spreader plate.

Usage of the heat spreader is obligatory, but there might be applications that require additional type of cooling solution together with heat spreader (passive casing heat dissipation or cooling fan). In any case, it is the system designer's responsibility to make sure that each device in the system operates within its specified thermal limits. The cooling solution should ensure that the thermal specifications for each component are met over the full operating range of the system.

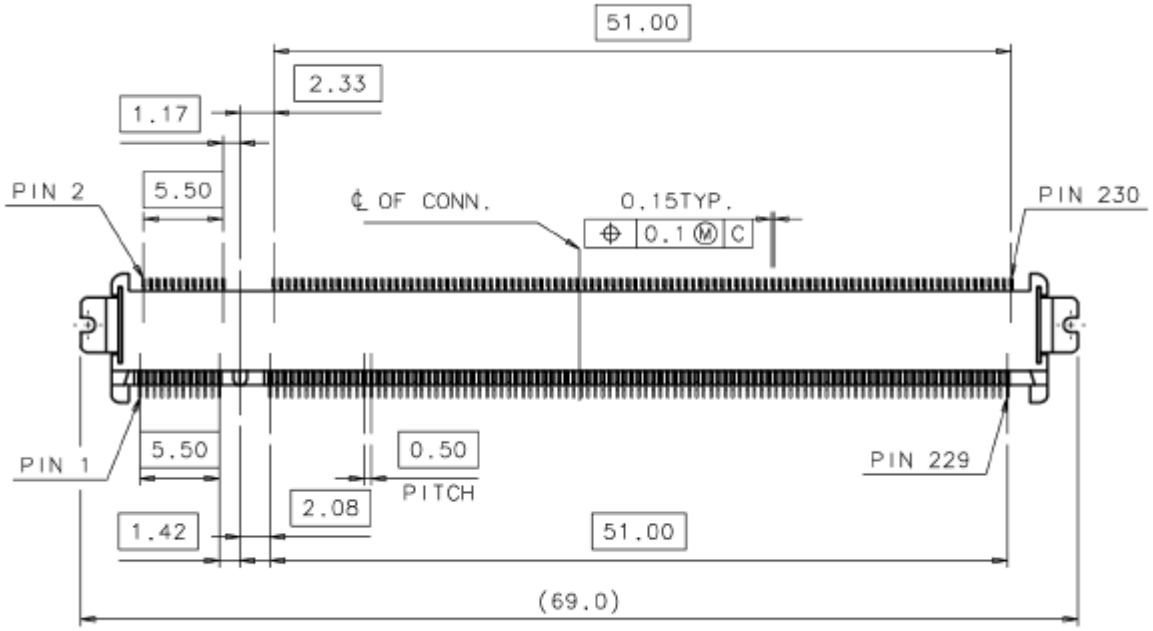




Bill of Material		
Pos-Nr.	**Description**	**Qty**
1	EPP-V7-DM8168™ HSP-001	1
2	Qseven® or V7 carrier board	1
3	EPP-V7-DM8168™	1
4	MEC Q7 COOLSTRIP ALU 70x5x5	1
5	MEC BOLT HEX-M/F M2.5 SW4 L5	2
6	MEC Screw Fillister Head M2.5x20 Cross	2
7	MEC Screw Fillister Head M2.5x6 Cross	2
8	MEC NUT HEX M2.5 SW5 m2.0	2

6 Connectors

6.1 MXM Connector Dimensions



6.2 MXM Connector Pin-Out

The following table shows the comparison between Qseven® pinout and both pinout modes supported by the EPP-V7-DM8168™ module (V7 mode and Qseven®-compatible mode). The pinout is automatically reconfigured depending on the type of carrier board in which the module is working.

Legend:
IO: Input/output; I: Input; O: Output; L: Output driven low; PD: Internal pull-down active; PU: Internal pull-up active; OD: Open drain; Z: High-Z; P: Power; NA: Not available (reserved).

Pin	Signal in Qseven® specification 2.0	Type	EPP-V7-DM8168™ signal in V7 mode	Type	EPP-V7-DM8168™ signal in Qseven®-compatibility mode	Type	Pin	Signal in Qseven® specification 2.0	Type	EPP-V7-DM8168™ signal in V7 mode	Type	EPP-V7-DM8168™ signal in Qseven®-compatibility mode	Type
1	GND	P	GND	P	GND	P	**2**	GND	P	GND	P	GND	P
3	GBE_MDI3-	IO	GBE0_MDI3-	IO	GBE_MDI3-	IO	**4**	GBE_MDI2-	IO	GBE0_MDI2-	IO	GBE_MDI2-	IO
5	GBE_MDI3+	IO	GBE0_MDI3+	IO	GBE_MDI3+	IO	**6**	GBE_MDI2+	IO	GBE0_MDI2+	IO	GBE_MDI2+	IO
7	GBE_LINK100#	O	GBE0_LINK100#	O	GBE_LINK100#	O	**8**	GBE_LINK1000#	O	GBE0_LINK1000#	O	GBE_LINK1000#	O
9	GBE_MDI1-	IO	GBE0_MDI1-	IO	GBE_MDI1-	IO	**10**	GBE_MDI0-	IO	GBE0_MDI0-	IO	GBE_MDI0-	IO
11	GBE_MDI1+	IO	GBE0_MDI1+	IO	GBE_MDI1+	IO	**12**	GBE_MDI0+	IO	GBE0_MDI0+	IO	GBE_MDI0+	IO
13	GBE_LINK#	O	GBE0_LINK#	O	GBE_LINK#	O	**14**	GBE_ACT#	O	GBE0_ACT#	O	GBE_ACT#	O
15	GBE_CTREF	P	GBE0_CTREF	P	GBE_CTREF	P	**16**	SUS_S5#	O	VIN[0]A_D[20] / VIN[0]B_DE	I	N/A	PU
17	WAKE#	I	WAKE#	I	WAKE#	I	**18**	SUS_S3#	O	SUS_S3#	O	SUS_S3#	O
19	SUS_STAT#	O	VIN[0]A_D[21] / VIN[0]B_FLD	I	N/A	PU	**20**	PWRBTN#	I	PWRBTN#	I	PWRBTN#	I
21	SLP_BTN#	I	VDAC_Y	O	N/A	Z	**22**	LID_BTN#	I	VDAC_C	O	N/A	Z
23	GND	P	GND	P	GND	P	**24**	GND	P	GND	P	GND	P
KEY													
25	GND	P	GND	P	GND	P	**26**	PWGIN	I	PWGIN	I	PWGIN	I
27	BATLOW#	I	EXT_INT2#	I	BATLOW#	I	**28**	RSTBTN#	I	RSTBTN#	I	RSTBTN#	I
29	SATA0_TX+	O	SATA0_TX+	O	SATA0_TX+	O	**30**	SATA1_TX+	O	SATA1_TX+	O	SATA1_TX+	O
31	SATA0_TX-	O	SATA0_TX-	O	SATA0_TX-	O	**32**	SATA1_TX-	O	SATA1_TX-	O	SATA1_TX-	O
33	SATA_ACT#	OD	SATA_ACT#	OD	SATA_ACT#	OD	**34**	GND	P	GND	P	GND	P
35	SATA0_RX+	I	SATA0_RX+	I	SATA0_RX+	I	**36**	SATA1_RX+	I	SATA1_RX+	I	SATA1_RX+	I
37	SATA0_RX-	I	SATA0_RX-	I	SATA0_RX-	I	**38**	SATA1_RX-	I	SATA1_RX-	I	SATA1_RX-	I
39	GND	P	GND	P	GND	P	**40**	GND	P	GND	P	GND	P
41	BIOS_DISABLE#	I	GBE1_ACT#	O	BIOS_DISABLE#	I	**42**	SDIO_CLK#	O	SDIO_CLK#	O	SDIO_CLK#	O
43	SDIO_CD#	IO	SDIO_CD#	IO	SDIO_CD#	IO	**44**	SDIO_LED	O	SDIO_LED	O	SDIO_LED	O
45	SDIO_CMD	IO	SDIO_CMD	IO	SDIO_CMD	IO	**46**	SDIO_WP	IO	SDIO_WP	IO	SDIO_WP	IO
47	SDIO_PWR#	O	SDIO_PWR#	O	SDIO_PWR#	O	**48**	SDIO_DAT1	IO	SDIO_DAT1	IO	SDIO_DAT1	IO
49	SDIO_DAT0	IO	SDIO_DAT0	IO	SDIO_DAT0	IO	**50**	SDIO_DAT3	IO	SDIO_DAT3	IO	SDIO_DAT3	IO
51	SDIO_DAT2	IO	SDIO_DAT2	IO	SDIO_DAT2	IO	**52**	SDIO_DAT5	IO	GBE1_CTREF	P	N/A	Z
53	SDIO_DAT4	IO	GBE1_MDI3-	IO	N/A	I	**54**	SDIO_DAT7	IO	GBE1_MDI2-	IO	N/A	I

55	SDIO_DAT6	IO	GBE1_MDI3+	IO	N/A	I	**56**	RSVD	NA	GBE1_MDI2+	IO	N/A	I
57	GND	P	GND	P	GND	P	**58**	GND	P	GND	P	GND	P
59	I2S_WS	O	I2S_WS/ MCA[2]_AFSX	O	I2S_WS	O	**60**	SMB_CLK /GP1_I2C_CLK	OD	GP0_I2C_CLK	OD	GP0_I2C_CLK	OD
61	I2S_RST#	O	I2S_RST#	O	I2S_RST#	O	**62**	SMB_DAT /GP1_I2C_DAT	OD	GP0_I2C_DAT	OD	GP0_I2C_DAT	OD
63	I2S_CLK	O	I2S_CLK/ MCA[2]_ACLKX	O	I2S_CLK	O	**64**	SMB_ALERT#	OD	EXT_INT1#	OD	SMB_ALERT#	OD
65	I2S_SDI	I	I2S_SDI/ MCA[2]_AXR[0]	I	I2S_SDI	I	**66**	GP0_I2C_CLK	OD	GP1_I2C_CLK	OD	GP1_I2C_CLK	OD
67	I2S_SDO	O	I2S_SDO/ MCA[2]_AXR[1]	O	I2S_SDO	O	**68**	GP0_I2C_DAT	OD	GP1_I2C_DAT	OD	GP1_I2C_DAT	OD
69	THRM#	I	VIN[0]A_D[22] / VIN[0]B_VSYNC	I	THRM#	I	**70**	WDTRIG#	I	VIN[0]A_D[23] / VIN[0]B_HSYNC	I	WDTRIG#	I
71	THRMTRIP#	O	MCA[2]_AHCLKX	IO	THRMTRIP#	O	**72**	WDOUT	O	VIN[0]A_FLD	I	WDOUT	O
73	GND	P	GND	P	GND	P	**74**	GND	P	GND	P	GND	P
75	USB_P7-/USB_SSTX0-	IO	GBE1_MDI1-	IO	N/A	I	**76**	USB_P6-/USB_SSRX0-	IO	GBE1_MDI0-	IO	N/A	I
77	USB_P7+/USB_SSTX0+	IO	GBE1_MDI1+	IO	N/A	I	**78**	USB_P6+/USB_SSRX0+	IO	GBE1_MDI0+	IO	N/A	I
79	USB_6_7_OC#	I	GBE1_LINK100#	O	N/A	Z	**80**	USB_4_5_OC#	I	GBE1_LINK1000#	O	N/A	Z
81	USB_P5-/USB_SSTX1-	IO	GBE1_LINK#	O	N/A	Z	**82**	USB_P4-/USB_SSRX1-	IO	VOUT[0]_G_Y_YC[3]	O	N/A	Z
83	USB_P5+/USB_SSTX1+	IO	VOUT[0]_G_Y_YC[2]	O	N/A	Z	**84**	USB_P4+/USB_SSRX1+	IO	VOUT[0]_G_Y_YC[5]	O	N/A	Z
85	USB_2_3_OC#	I	VOUT[0]_G_Y_YC[4]	O	N/A	Z	**86**	USB_0_1_OC#	I	USB_0_1_OC#	I	USB_0_1_OC#	I
87	USB_P3-	IO	VOUT[0]_G_Y_YC[6]	O	N/A	Z	**88**	USB_P2-	IO	VOUT[0]_G_Y_YC[7]	O	N/A	Z
89	USB_P3+	IO	VOUT[0]_G_Y_YC[8]	O	N/A	Z	**90**	USB_P2+	IO	VOUT[0]_G_Y_YC[9]	O	N/A	Z
91	USB_CC	I	USB_CC	I	USB_CC	I	**92**	USB_ID	I	VIN[0]A_DE	I	N/A	I
93	USB_P1-	IO	USB_P1-	IO	USB_P1-	IO	**94**	USB_P0-	IO	USB_P0-	IO	USB_P0-	IO
95	USB_P1+	IO	USB_P1+	IO	USB_P1+	IO	**96**	USB_P0+	IO	USB_P0+	IO	USB_P0+	IO
97	GND	P	GND	P	GND	P	**98**	GND	P	GND	P	GND	P
99	eDP0_TX0+/LVDS_A0+	O	VOUT[0]_B_CB_C[2]	O	N/A	L	**100**	eDP1_TX0+/LVDS_B0+	O	VOUT[0]_B_CB_C[3]	O	N/A	L
101	eDP0_TX0-/LVDS_A0-	O	VOUT[0]_B_CB_C[4]	O	N/A	L	**102**	eDP1_TX0-/LVDS_B0-	O	VOUT[0]_B_CB_C[5]	O	N/A	L
103	eDP0_TX1+/LVDS_A1+	O	VOUT[0]_B_CB_C[6]	O	N/A	L	**104**	eDP1_TX1+/LVDS_B1+	O	VOUT[0]_B_CB_C[7]	O	N/A	L
105	eDP0_TX1-/LVDS_A1-	O	VOUT[0]_B_CB_C[8]	O	N/A	L	**106**	eDP1_TX1-/LVDS_B1-	O	VOUT[0]_B_CB_C[9]	O	N/A	L
107	eDP0_TX2+/LVDS_A2+	O	GND	P	GND	P	**108**	eDP1_TX2+/LVDS_B2+	O	GND	P	GND	P
109	eDP0_TX2-/LVDS_A2-	O	VOUT[0]_CLK	O	N/A	L	**110**	eDP1_TX2-/LVDS_B2-	O	VOUT[0]_HSYNC	O	N/A	L
111	LVDS_PPEN	O	VOUT[0]_FLD	O	N/A	L	**112**	LVDS_BLEN	O	VOUT[0]_VSYNC	O	N/A	L
113	eDP0_TX3+/LVDS_A3+	O	VIN[0]A_D[0]	I	N/A	IPD	**114**	eDP1_TX3+/LVDS_B3+	O	VIN[0]A_D[1]	I	N/A	IPD

115	eDP0_TX3-/LVDS_A3-	O	VIN[0]A_D[2]	I	N/A	IPD	**116**	eDP1_TX3-/LVDS_B3-	O	VIN[0]A_D[3]	I	N/A	IPD
117	GND	P	GND	P	GND	P	**118**	GND	P	GND	P	GND	P
119	eDP0_AUX+/LVDS_A_CLK+	O	VIN[0]A_D[4]	I	N/A	IPD	**120**	eDP1_AUX+/LVDS_B_CLK+	O	VIN[0]A_D[5]	I	N/A	IPD
121	eDP0_AUX-/LVDS_A_CLK-	O	VIN[0]A_D[6]	I	N/A	IPD	**122**	eDP1_AUX-/LVDS_B_CLK-	O	VIN[0]A_D[7]	I	N/A	IPD
123	LVDS_BLT_CTRL/GP_PWM_OUT0	O	VIN[0]A_D[8]	I	N/A	IPD	**124**	GP_1-Wire_Bus	IO	VIN[0]A_D[9]	I	N/A	I
125	GP2_I2C_DAT/LVDS_DID_DAT	OD	GND	P	GND	P	**126**	eDP0_HPD#/LVDS_BLC_DAT	OD	GND	P	GND	P
127	GP2_I2C_CLK/LVDS_DID_CLK	OD	VIN[0]A_D[10]	I	N/A	IPU	**128**	eDP1_HPD#/LVDS_BLC_CLK	OD	VIN[0]A_D[11]	I	N/A	IPU
129	CAN0_TX	O	VIN[0]A_D[12]	I	N/A	IPD	**130**	CAN0_RX	I	VIN[0]A_D[13]	I	N/A	Z
131	DP_LANE3+/TMDS_CLK+	O	DP_LANE3+/TMDS_CLK+	O	DP_LANE3+/TMDS_CLK+	O	**132**	RSVD (diff pair)	I	VIN[0]A_D[14]	I	N/A (diff pair)	I
133	DP_LANE3-/TMDS_CLK-	O	DP_LANE3-/TMDS_CLK-	O	DP_LANE3-/TMDS_CLK-	O	**134**	RSVD (diff pair)	I	VIN[0]A_D[15]	I	N/A (diff pair)	I
135	GND	P	GND	P	GND	P	**136**	GND	P	GND	P	GND	P
137	DP_LANE1+/TMDS_LANE1+	O	DP_LANE1+/TMDS_LANE1+	O	DP_LANE1+/TMDS_LANE1+	O	**138**	DP_AUX+	IO	VIN[0]A_CLK	I	N/A	IPD
139	DP_LANE1-/TMDS_LANE1-	O	DP_LANE1-/TMDS_LANE1-	O	DP_LANE1-/TMDS_LANE1-	O	**140**	DP_AUX-	IO	VIN[0]A_HSYNC	I	N/A	IPD
141	GND	P	GND	P	GND	P	**142**	GND	P	GND	P	GND	P
143	DP_LANE2+/TMDS_LANE0+	O	DP_LANE2+/TMDS_LANE0+	O	DP_LANE2+/TMDS_LANE0+	O	**144**	RSVD (diff pair)	I	VIN[0]A_VSYNC	I	N/A (diff pair)	I
145	DP_LANE2-/TMDS_LANE0-	O	DP_LANE2-/TMDS_LANE0-	O	DP_LANE2-/TMDS_LANE0-	O	**146**	RSVD (diff pair)	I	VIN[0]B_CLK	I	N/A (diff pair)	I
147	GND	P	GND	P	GND	P	**148**	GND	P	GND	P	GND	P
149	DP_LANE0+/TMDS_LANE2+	O	DP_LANE0+/TMDS_LANE2+	O	DP_LANE0+/TMDS_LANE2+	O	**150**	HDMI_CTRL_DAT	OD	HDMI_CTRL_DAT	OD	HDMI_CTRL_DAT	OD
151	DP_LANE0-/TMDS_LANE2-	O	DP_LANE0-/TMDS_LANE2-	O	DP_LANE0-/TMDS_LANE2-	O	**152**	HDMI_CTRL_CLK	OD	HDMI_CTRL_CLK	OD	HDMI_CTRL_CLK	OD
153	DP_HDMI_HPD#	I	DP_HDMI_HPD#	I	DP_HDMI_HPD#	I	**154**	RSVD	I	VIN[0]A_D[18]/VIN[1]A_FLD	I	N/A	I
155	PCIE_CLK_REF+	O	PCIE_CLK_REF+	O	PCIE_CLK_REF+	O	**156**	PCIE_WAKE#	I	PCIE_WAKE#	I	PCIE_WAKE#	I
157	PCIE_CLK_REF-	O	PCIE_CLK_REF-	O	PCIE_CLK_REF-	O	**158**	PCIE_RST#	O	PCIE_RST#	O	PCIE_RST#	O
159	GND	P	GND	P	GND	P	**160**	GND	P	GND	P	GND	P
161	PCIE3_TX+	O	VIN[0]A_D[16] / VIN[1]A_HSYNC	I	N/A	IPD	**162**	PCIE3_RX+	I	VIN[1]A_CLK	I	N/A	Z
163	PCIE3_TX-	O	VIN[0]A_D[17] / VIN[1]A_VSYNC	I	N/A	IPD	**164**	PCIE3_RX-	I	VIN[1]B_CLK	I	N/A	Z
165	GND	P	GND	P	GND	P	**166**	GND	P	GND	P	GND	P
167	PCIE2_TX+	O	VIN[1]A_D[0]	I	N/A	IPD	**168**	PCIE2_RX+	I	VIN[1]A_D[1]	I	N/A	Z
169	PCIE2_TX-	O	VIN[1]A_D[2]	I	N/A	IPD	**170**	PCIE2_RX-	I	VIN[1]A_D[3]	I	N/A	Z
171	UART0_TX	O	UART0_TX	O	UART0_TX	O	**172**	UART0_RTS#	O	VIN[1]A_D[4]	I	N/A	OPD

173	PCIE1_TX+	O	PCIE1_TX+	O	PCIE1_TX+	O	**174**	PCIE1_RX+	I	PCIE1_RX+	I	PCIE1_RX+	I
175	PCIE1_TX-	O	PCIE1_TX-	O	PCIE1_TX-	O	**176**	PCIE1_RX-	I	PCIE1_RX-	I	PCIE1_RX-	I
177	UART0_RX	IPU	UART0_RX	IPU	UART0_RX	IPU	**178**	UART0_CTS#	I	VIN[1]A_D[5]	I	N/A	I
179	PCIE0_TX+	O	PCIE0_TX+	O	PCIE0_TX+	O	**180**	PCIE0_RX+	I	PCIE0_RX+	I	PCIE0_RX+	I
181	PCIE0_TX-	O	PCIE0_TX-	O	PCIE0_TX-	O	**182**	PCIE0_RX-	I	PCIE0_RX-	I	PCIE0_RX-	I
183	GND	P	GND	P	GND	P	**184**	GND	P	GND	P	GND	P
185	LPC_AD0/GPIO0	IO	VIN[1]A_D[6]	I	N/A	IPD	**186**	LPC_AD1/GPIO1	IO	VIN[1]A_D[7]	I	N/A	IPD
187	LPC_AD2/GPIO2	IO	VIN[1]A_D[8]	I	N/A	IPD	**188**	LPC_AD3/GPIO3	IO	VIN[1]A_D[9]	I	N/A	IPD
189	LPC_CLK/GPIO4	IO	VIN[1]A_D[10]	I	N/A	IPD	**190**	LPC_FRAME#/GPIO5	IO	VIN[1]A_D[11]	I	N/A	IPD
191	SERIRQ/GPIO6	IO	VIN[1]A_D[12]	I	N/A	IPD	**192**	LPC_LDRQ#/GPIO7	IO	VIN[1]A_D[13]	I	N/A	IPD
193	VCC_RTC	P	VCC_RTC	P	VCC_RTC	P	**194**	SPKR/GP_PWM_OUT2	O	VIN[1]A_D[14]	I	N/A	I
195	FAN_TACHOIN/GP_TIMER_IN	I	VIN[1]A_D[15]	I	N/A	I	**196**	FAN_PWMOUT/GP_PWM_OUT1	O	VIN[0]A_D[19] / VIN[1]A_DE[0]	I	N/A	I
197	GND	P	GND	P	GND	P	**198**	GND	P	GND	P	GND	P
199	SPI_MOSI	O	SPI_MOSI	O	SPI_MOSI	O	**200**	SPI_CS0#	O	SPI_CS0#	O	SPI_CS0#	O
201	SPI_MISO	I	SPI_MISO	I	SPI_MISO	I	**202**	SPI_CS1#	O	SPI_CS1#	O	SPI_CS1#	O
203	SPI_SCK	O	SPI_SCK	O	SPI_SCK	O	**204**	MFG_NC4	NC	JTAG_TRST# / MFG_SEL	I	JTAG_TRST# / MFG_SEL	I
205	VCC_5V_SB	P	VCC_5V_SB	P	VCC_5V_SB	P	**206**	VCC_5V_SB	P	VCC_5V_SB	P	VCC_5V_SB	P
207	MFG_NC0	NC	JTAG_TCLK	I	JTAG_TCLK	I	**208**	MFG_NC2	NC	JTAG_TDI / UART1_RX	I	JTAG_TDI / UART1_RX	I
209	MFG_NC1	NC	JTAG_TDO / UART1_TX	O	JTAG_TDO / UART1_TX	O	**210**	MFG_NC3	NC	JTAG_TMS	I	JTAG_TMS	I
211	VCC	P	VCC	P	VCC	P	**212**	VCC	P	V7_MODE#	IPD	N/A	Z
213	VCC	P	VCC	P	VCC	P	**214**	VCC	P	VCC	P	VCC	P
215	VCC	P	VCC	P	VCC	P	**216**	VCC	P	VCC	P	VCC	P
217	VCC	P	VCC	P	VCC	P	**218**	VCC	P	VCC	P	VCC	P
219	VCC	P	VCC	P	VCC	P	**220**	VCC	P	VCC	P	VCC	P
221	VCC	P	VCC	P	VCC	P	**222**	VCC	P	VCC	P	VCC	P
223	VCC	P	VCC	P	VCC	P	**224**	VCC	P	VCC	P	VCC	P
225	VCC	P	VCC	P	VCC	P	**226**	VCC	P	VCC	P	VCC	P
227	VCC	P	VCC	P	VCC	P	**228**	VCC	P	VCC	P	VCC	P
229	VCC	P	VCC	P	VCC	P	**230**	VCC	P	VCC	P	VCC	P